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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,569	09/30/2003	Shigeru Morimoto	MTS-3463US	7911
23122	7590	11/03/2006	EXAMINER	
RATNERPRESTIA P O BOX 980 VALLEY FORGE, PA 19482-0980			NORRIS, JEREMY C	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/676,569

Applicant(s)

MORIMOTO ET AL

Examiner

Jeremy C. Norris

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 3,9-11,13 and 14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-7 and 12 is/are rejected.
- 7) ☒ Claim(s) 4 and 8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 09/03,09/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Election/Restrictions***

Applicant's election without traverse of Species ia, claims 1, 2, 4-8, and 12 in the reply filed on 16 August 2006 is acknowledged.

***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 states the limitation "wherein said current-carrying element is formed between predetermined layers between said first connection point and said second end and is connected to the conductive part of said via hole instead of being connected to said second end." However, via dependency from claim 1, the current carry element is necessarily located at the second end, thus, this additional limitation is in direct conflict with the previously stated limitation which results in a device that the ordinarily skilled artisan would not know how to make and use. Furthermore, since this limitation results in a physical impossibility, the limitation is deemed to not further limit claim 1 from which claim 7 depends and has been treated as such when evaluated with the prior art.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 6, 7, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 63-59003 (Nishimura).

Nisimura discloses, referring primarily to figure 3, a printed circuit board having: a multilayer substrate (11); a via hole (6) penetrating said multilayer substrate; a surface wiring (1) wired on the surface of said multilayer substrate and connected to a first end which is one end of said via hole; at least one inner layer wiring (4) formed inside said multilayer substrate and connected to a portion other than upper and lower ends of a conductive part of said via hole; and a current-carrying element (7) connected to a second end having no said surface wiring connected thereto on an opposite side to said first end of the conductive part of said via hole; and wherein: said current-carrying element has an electrical length by which a value of an impedance at a predetermined frequency is larger than a predetermined value on seeing said current-carrying element side from a first connection point closest to said second end, of the connection points between said inner layer wiring and the conductive part of said via hole; and said predetermined value is the value of the impedance at the predetermined frequency on seeing said second end side from said first connection point in the case where said current-carrying element does not exist (see abstract) [claims 1, 7], wherein a

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part of said current-carrying element is formed by at least one via hole [claim 5], wherein a shape of said current-carrying element is substantially a sector [claim 6].

Similarly, Nishimura discloses, a method of manufacturing a printed circuit board having: a step of connecting a current-carrying element (7) to a second end having no surface wiring connected thereto on an opposite side to a first end of a via hole (6) penetrating a multilayer substrate (11) and having a surface wiring (1) connected to said first end of a conductive part thereof; and a step of determining an electrical length of said current-carrying element so that a value of an impedance at a predetermined frequency on seeing said current-carrying element side from a first connection point closest to said second end, of connection points between at least one inner layer wiring connected to a portion other than said first end and said second end of the conductive part of said via hole and formed inside said multilayer substrate and the conductive part of said via hole, is higher than a predetermined value, and wherein: said predetermined value is the value of the impedance at said predetermined frequency on seeing said second end side from said first connection point in the case where said current-carrying element does not exist (see abstract) [claim 12].

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of US 6,269,240 B1 (Chong).

Nishimura discloses the claimed invention as described above including that the end of the current carrying element is open. Nishimura does not specifically state that the total of the electrical length from said first connection point to said second end and the electrical length of said current-carrying element is substantially  $n/2$  times ( $n$  is a natural number) a wavelength corresponding to said predetermined frequency [claim 2]. However, it is well known in the art to form conductors with an electrical length of half a

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wavelength to reduce losses due to reflection as evidenced by Chong (col. 5, lines 55-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to form the current carrying element in the invention of Nishimura with an electrical length of half a wavelength as is known in the art and evidenced by Chong. The motivation for doing so would have been to reduce signal losses due to reflection.

### ***Allowable Subject Matter***

Claims 4 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 4 states the limitation "wherein a part of said current-carrying element is formed by a chip inductor". This limitation, in conjunction with the other claimed features, was neither found to be disclosed in, nor suggested by the prior art. Claim 8 states the limitation "the end of said current-carrying element and the end of said other current-carrying element are mutually connected". This limitation, in conjunction with the other claimed features, was neither found to be disclosed in, nor suggested by the prior art.

### ***Conclusion***

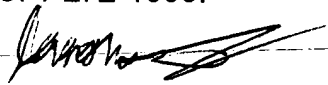
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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JCSN